

# TOSHIBA MOS MEMORY PRODUCTS

1024 WORD x 4 BIT STATIC RAM

N CHANNEL SILICON GATE DEPLETION LOAD

TMM314AP

TMM314AP-I

TMM314AP-3

TMM314APL

TMM314APL-I

TMM314APL-3

## DESCRIPTION

TMM314AP family is 1024 word x 4 bit high speed read write memories operated with 5 V single power supply. The memories with 6 Tr. cells are static in operation and require no clocks or refresh period and suitable for use in microprocessor application systems where high performance, low cost, simple interfacing are important design objectives.

TMM314AP family is able to be connected to

## FEATURES

- Fully decoded 1024 word x 4 bit organization
- Static operation — No clocks or refresh period
- Single 5V supply voltage —  $V_{CC} = 5V \pm 10\%$
- Easy memory expansion — CS input
- Three state output — Wired OR tie capability
- Inputs and outputs directly TTL compatible
- Data input/output terminal is common
- Input protected — All inputs have protection against static charge
- 2114 Type Pin compatible

TTL directly and to drive 1 STTL or 5 LSTTLs.

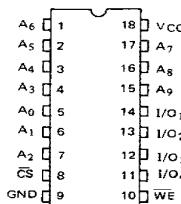
TMM314AP family is fabricated with N channel silicon gate depletion load type MOS technology by ion implantation for fast speed, stable performance and reliability.

The chip is moulded in the standard 18 pin plastic package of 0.3 inch width for low cost and high density assembly.

- Low Power dissipation and Access time  
Power and Access time (maximum value)

	Access time	Power
TMM314AP-1	200 ns	550 mW
TMM314AP-3	300 ns	550 mW
TMM314AP	450 ns	550 mW
TMM314APL-1	200 ns	385 mW
TMM314APL-3	300 ns	385 mW
TMM314APL	450 ns	385 mW

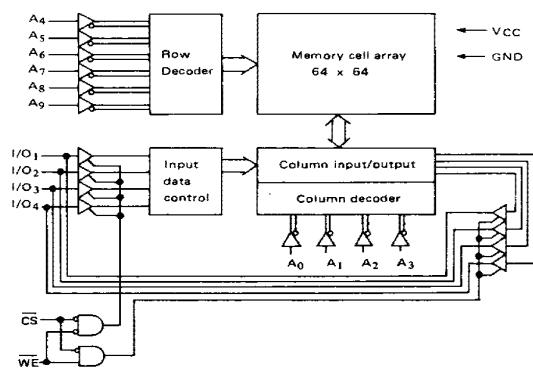
## PIN CONNECTION (TOP VIEW)



## PIN NAMES

A <sub>0</sub> ~ A <sub>3</sub>	Column Address Inputs
A <sub>4</sub> ~ A <sub>9</sub>	Row Address Inputs
I/O <sub>1</sub> ~ I/O <sub>4</sub>	Data Input/Output
CS	Chip Select Input
WE	Write Enable Input
VCC	Supply Voltage
GND	Ground

## BLOCK DIAGRAM



**MAXIMUM RATINGS**

SYMBOL	ITEM	RATING	UNIT
VCC	Supply Voltage	-0.5 ~ 7.0	V
VI/O	Input/Output Voltage	-0.5 ~ 7.0	V
TOPR	Operating Temperature	0 ~ 70	°C
TSTG	Storage Temperature	-55 ~ 150	°C
TSOLDER	Soldering Temperature - Time	260 ~ 10	°C . sec
PD	Power dissipation (Ta = 70°C)	850	mW

**DC RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIH	Input High Voltage	—	2.0	—	VCC	V
VIL	Input Low Voltage	—	-0.5	—	0.8	V
VCC	Supply Voltage	—	4.5	5	5.5	V

**DC CHARACTERISTICS (Ta = 0 ~ 70°C)**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.*	MAX.	UNIT
I <sub>IH</sub>	Input High Current	V <sub>IN</sub> = 5.50 V	—	—	10	μA
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = 0 V	—	—	-10	μA
V <sub>OH</sub>	Output High Voltage	I <sub>SOURCE</sub> = -1.0 mA	2.4	2.8	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>SINK</sub> = 2.1 mA	—	0.15	0.4	V
I <sub>OH</sub>	Output High Current	V <sub>OUT</sub> = 2.4 V	-1.0	-5.5	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OUT</sub> = 0.4 V	2.1	6.5	—	mA
I <sub>LO</sub>	Output Leakage Current	CE = V <sub>IH</sub> or WE = V <sub>IL</sub> V <sub>OUT</sub> = 0.4 V ~ VCC	—	—	± 10	μA
I <sub>CC1</sub>	Supply Current	TMM314A PL/PL-1/PL-3 I <sub>OUT</sub> = 0 mA	25°C 0°C	50 —	64 70	mA
I <sub>CC2</sub>	Supply Current	TMM314A P/P-1/P-3 I <sub>OUT</sub> = 0 mA	25°C 0°C	70 —	90 100	mA

\* Ta = 25°C, V<sub>CC</sub> = 5V

**AC CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 10%, CL = 100pF, tr, tf ≤ 10 ns)****READ CYCLE**

SYMBOL	PARAMETER	TMM314AP-1/APL-1		TMM314AP-3/APL-3		TMM314AP/APL		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	200	—	300	—	450	—	ns
t <sub>AC</sub>	Access Time	—	200	—	300	—	450	ns
t <sub>CS</sub>	Chip Select Time	—	70	—	100	—	100	ns
t <sub>CX</sub>	Output Active from CS	20	—	20	—	20	—	ns
t <sub>D</sub>	Chip Deselect Time	0	40	0	80	0	100	ns
t <sub>OH</sub>	Output Hold from Address Change	20	—	20	—	20	—	ns

**WRITE CYCLE**

SYMBOL	PARAMETER	TMM314AP-1/APL-1		TMM314AP-3/APL-3		TMM314AP/APL		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	200	—	300	—	450	—	ns
t <sub>WP</sub>	Write Pulse Width	120	—	150	—	200	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	ns
t <sub>ODW</sub>	Output High Z from WE	0	40	0	80	0	100	ns
t <sub>DS</sub>	Data Setup Time	120	—	150	—	200	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	ns
t <sub>AW</sub>	Address to Write Setup Time	30	—	30	—	30	—	ns

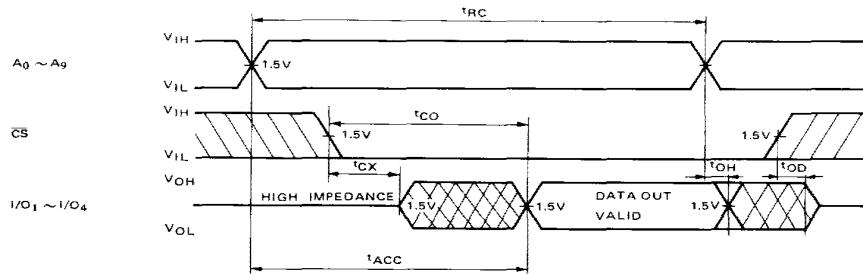
**CAPACITANCE (Ta = 25°C, f = 1 MHz)**

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		V <sub>IN</sub> = AC Ground	V <sub>OUT</sub> = AC Ground				
C <sub>IN</sub>	Input Capacitance	—	—	—	—	5	pF
C <sub>OUT</sub>	Output Capacitance	—	—	—	—	5	pF

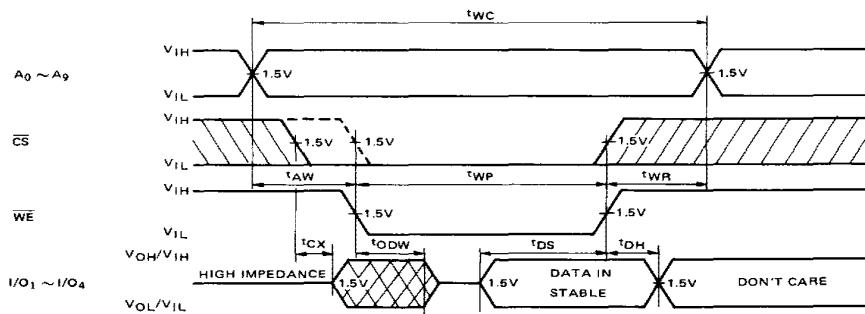
Note: This parameter is periodically sampled and not 100% tested.

## TIMING WAVEFORMS

## READ CYCLE



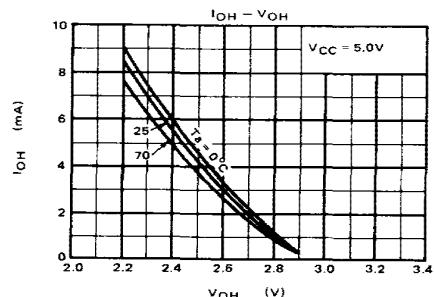
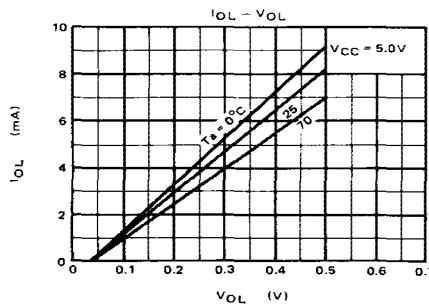
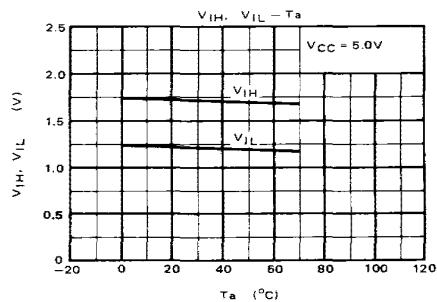
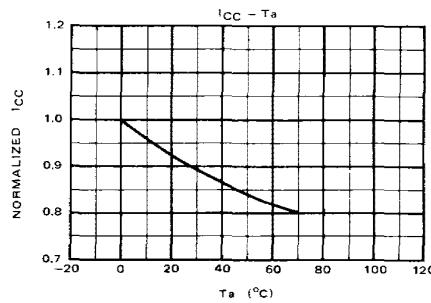
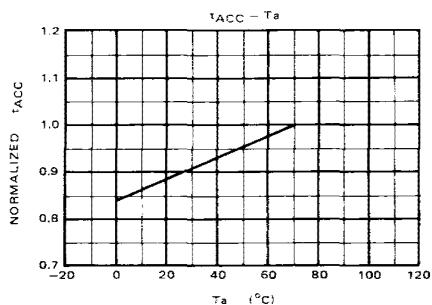
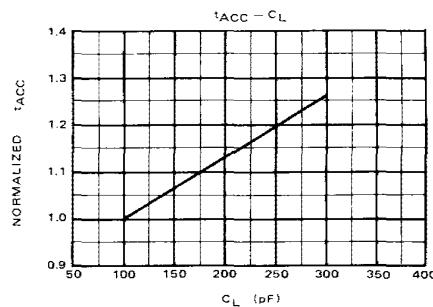
## WRITE CYCLE



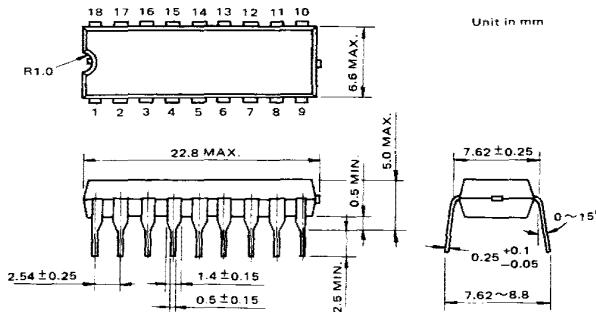
Note 1 : WE is high for a READ CYCLE.

2 :  $t_{WP}$  is measured from the latter of CS or WE going low to the earlier of CS or WE going high.

## TYPICAL CHARACTERISTICS



## OUTLINE DRAWINGS



**Notes:** Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 18 leads.

**Note:** Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.  
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